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In digital circuit design, register-transfer level is a design abstraction which models a synchronous digital circuit in terms of the flow of digital signals between hardware registers, and the logical operations

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performed on those signals. Register-transfer-level abstraction is used in hardware description languages like Verilog and VHDL to create high-level representations of a circuit, from which lower-level representations and ultimately actual wiring can be derived. Design at the RTL level

~~Register transfer level - Wikipedia~~

A student exposed to RTL design in a first course will have a more relevant view of the modern digital design field, leading not only to a better appreciation of modern computers and other digital devices, but to a more accurate understanding of careers involving digital design.

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Register Transfer Level (RTL) is an abstraction for defining the digital portions of a design. It is the principle abstraction used for defining electronic systems today and often serves as the golden model in the design and verification flow. The RTL design is usually captured using a hardware description language (HDL) such as Verilog or VHDL.

~~Register Transfer Level (RTL) — Semiconductor Engineering~~

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Logic design is a step in the standard design cycle in which the functional design of an electronic circuit is converted into the representation which captures logic operations, arithmetic operations, control flow, etc. A common output of this step is RTL description. Logic design is commonly followed by the circuit design step.

Logic synthesis — Wikipedia

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